G06F 1/32

(12) UK Patent Application (19) GB (11) 2 235 797 (13) A

(43) Date of A publication 13.03.1991

(21) Application No 9018259.3

(22) Date of filing 20.08.1990

(30) Priority data
(31) 405637 (32) 08.09.1989 (33) US

(51) INT CL[5]
G06F 1/32

(52) UK CL (Edition K)
G4A ASX

(56) Documents cited
US 4698748 A

(58) Field of search
UK CL (Edition K) G4A ASX
INT CL[5] G06F

(71) Applicant
Apple Computer Inc

(Incorporated in the USA – California)

20525 Mariani Avenue, Cupertino, California 95014, United States of America

(72) Inventors
R Steven Smith
Mike S. Hanlon
Robert L. Bailey

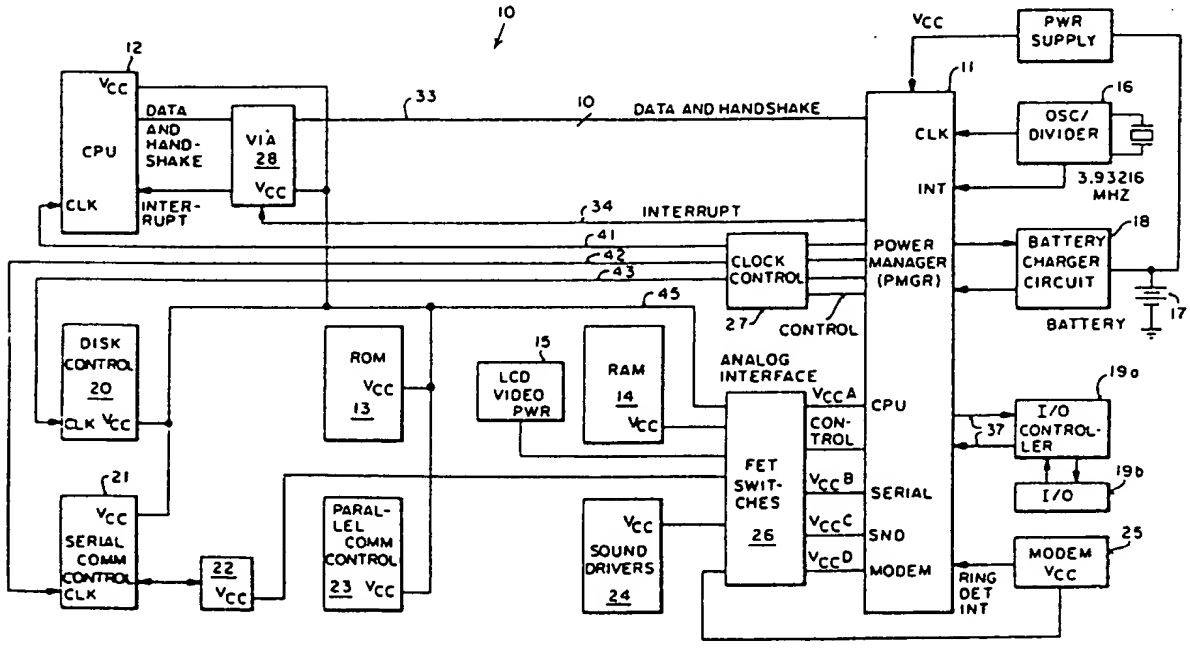
(74) Agent and/or Address for Service
Potts Kerr and Co
15 Hamilton Square, Birkenhead, Merseyside, L41 6BR, United Kingdom

DOC

(54) Power management for a portable computer

(57) A power manager (PMGR) within a portable laptop computer provides power (via 26) and clocking control (via 27) to various units within the computer in order to conserve battery power. Transistor switches controlled by the power manager control the distribution of power and clock signals to the various units within the computer. The power manager includes a software routine for continually monitoring various units and when certain units are either not needed and/or not currently in use, power and/or clock signals are removed from a given unit, and the computer can be switched between three modes viz. normal, slow and sleep.

FIG 1



At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

GB 2 235 797 A

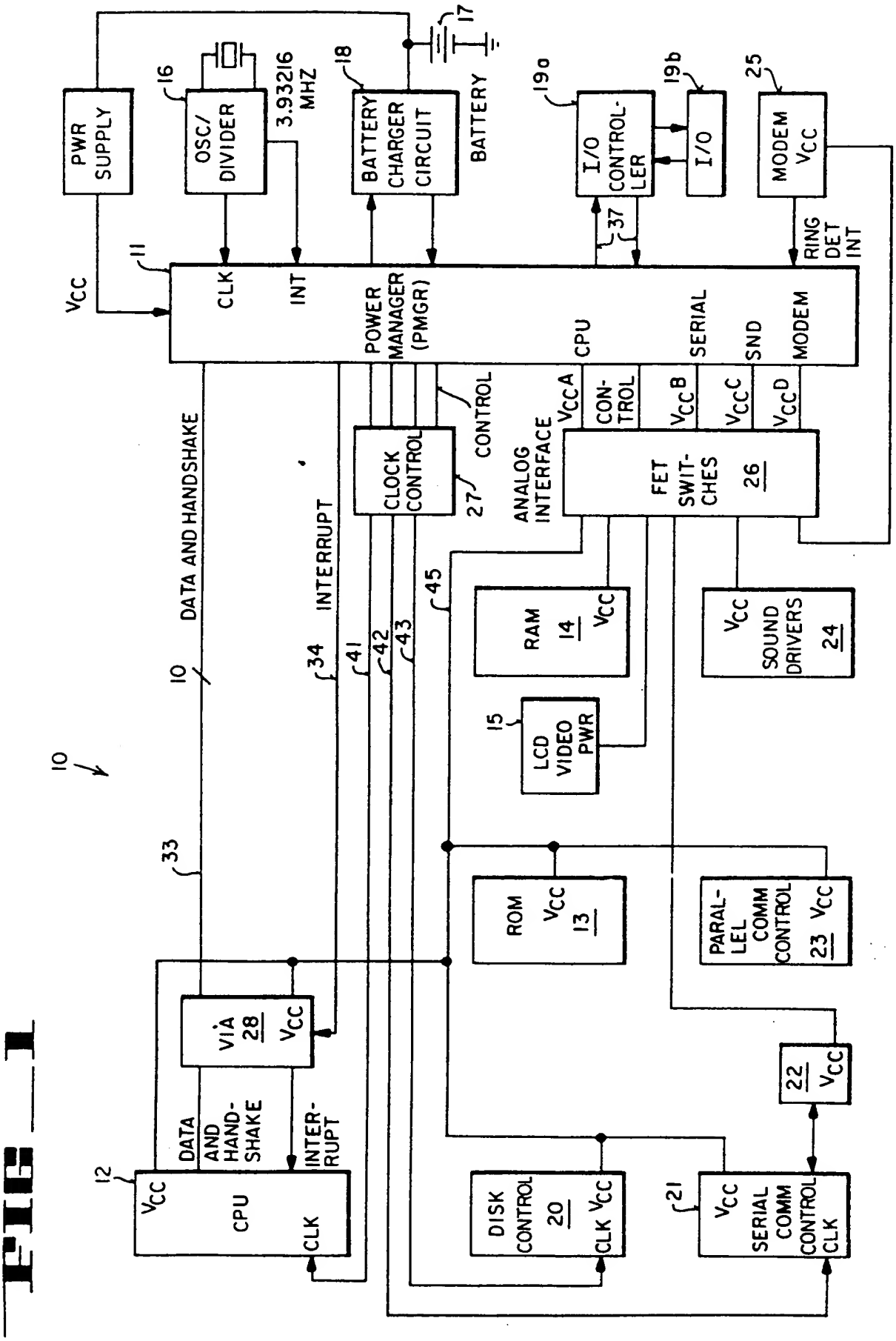

10
PWR SUPPLY
OSC/ DIVIDER
16
3.93216 MHZ
BATTERY CHARGER CIRCUIT
18
17
BATTERY
19a
I/O CONTROL-LER
19b
I/O
25
MODEM Vcc
RING DET INT
37
11
Vcc
CLK
INT
POWER MANAGER (PMGR)
CPU
SERIAL
SND
MODEM
CONTROL
Vcc A
CON-TROL
Vcc B
Vcc C
Vcc D
CLOCK CONTROL
27
ANALOG INTERFACE
FET SWIT-CHES 26
DATA AND HANDSHAKE
10
INTERRUPT
34
41
42
43
45
RAM 14 Vcc
Vcc SOUND DRIVERS 24
15
LCD VIDEO PWR
33
ROM Vcc 13
PARAL-LEL COMM CONTROL 23 Vcc
VIA 28 Vcc
22 Vcc
DATA AND HAND-SHAKE
INTER-RUPT
12
Vcc
CPU
CLK
DISK CONTROL 20
CLK Vcc
21
Vcc
SERIAL COMM CONTROL
CLK

FIG_1

POWER MANAGEMENT FOR A LAPTOP COMPUTER.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a power distribution scheme in a portable computer and, more specifically, to power management in a laptop computer.

2. Prior Art

Power consumption in an electronic device is always a significant concern and a power supply must be designed to adequately power the device. Aside from the capability of the power supply to provide ample power to power the corresponding device, heat dissipation, physical size, weight, efficiency, and other related characteristics are paramount in designing or selecting the power source. These characteristics become exceptionally critical when the device the power supply is to support is a self-sufficient portable unit.

In many portable units, a self-supporting power source, such as a battery, is used to provide the power when the unit is decoupled from its main or external power source, such as 110 Volt AC (ordinary house current). Typically a battery is used to provide the independent and portable power source. In some instances the battery functions as an auxiliary power source to maintain certain critical circuits active, such as keeping the memory alive to retain any information stored in the memory. In other instances, the battery functions as the main power source to fully power the device.

In the area of information processing, miniaturization of processing devices has permitted the portability of computing devices. One of the first such portable processing devices was a hand held calculator, wherein the calculator operated from a battery power source and could easily be carried about by the user. The battery would power all of the functions of the calculator

However, as the personal desk top computer systems are made portable, it is desirable to provide a computer which contains a fully contained power source so that the computer is completely portable. These self - sufficient computer systems are typically referred to as laptops (because of the small physical size and light weight) and are designed to operate for a certain number of hours from its internal power source, which is typically a battery. Although a variety of the portable calculator technology can be implemented within such a laptop, additional constraints are placed in that the additional circuitry, memory, viewing screen and any peripheral devices attached to the system will necessarily consume additional power. In order to extend the self-sustaining time period of these laptops while keeping the battery size and weight to a minimum, a sophisticated power management scheme is required to provide power only to those circuits and devices which require such power and to remove power, or at least to make a given circuit enter a low power consumption mode, when that circuit is not needed. The management scheme must also continually monitor the various circuits and devices in order that power can be applied immediately to activate such circuits and devices when needed.

The present invention provides for such a power management apparatus for a laptop computer in order to extend the self-sustaining time period so that the laptop computer can operate for an extended period of time once external power is disconnected.

3. Prior Art References

A number of prior art references are known for monitoring and controlling the consumption of power to a device or to a portion of a device including a means of providing a timeout when user interaction has not occurred for a given time period. However, these references pertain to the simpler calculator technology or to portions of a computer system and fail to disclose the

SUMMARY OF THE INVENTION

The present invention describes a power manager for use in a laptop computer. The laptop computer is a fully self-sufficient computer which is powered by an internal battery when the computer is disconnected from an external power source. Because power conservation is paramount to sustain the computer as long as possible from the internal battery, a power manager is provided to monitor and control various circuit operations. Various units of the computer, including peripheral units, generally function equivalently to well-known personal desktop computers. However, the power source to the various devices are controlled by the power manager and a plurality of transistor switches are used to switch the power source to the various devices. The operation of these switches is controlled by the power manager. Additionally, various clock signals are also coupled through switches which are controlled by the power manager so that the clock signals can be disconnected from certain units of the computer.

The power manager continually monitors various circuit functions such that devices not in use have their power sources or clock signals disconnected in order to deactivate devices to conserve battery power. The removal of clock signals from those units having clock control places these various units into an inactive state. However, because power is still applied to these units, various internal states retain their current state until the clock signal is restored.

The power manager is capable of operating in one of three modes of operation. In a first mode the computer operates in a normal active mode where most of the units are active at all times and/or some of the other units are caused to be made active when needed. A second state is a sleep state in which the computer enters into an inactive state and the power manager continues to monitor various circuit conditions. When a certain predetermined

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a circuit block diagram of the various units of the laptop computer and showing power lines, clock signal lines and control lines pertaining to the power management scheme of the present invention.

Figure 2 is a circuit schematic diagram showing an example of a transistor switch utilized to control the switching of a clock signal to a given device.

Figure 3 is a circuit schematic diagram showing an example of a transistor switch utilized to control the switching of power to a given device.

Several additional units are included within computer 10 to operate with the PMGR unit 11. Analog interface unit 26, clock control unit 27 and an internal interface unit, referred to as a via unit 28, are included to function in conjunction with the PMGR 11. It is to be appreciated that units 12-25 are devices used in prior art computers and such description and operation of these units are not included herein. Units 12-25, except for unit 17 and 18, are available with the Macintosh™ brand computers of Apple Computer Inc., of Cupertino, California.

In functional terms, CPU 12 is the main processing unit for computer 10 and in the preferred embodiment is a 68000 based (part numbers 68000, 68020 and 68030) processor manufactured by Motorola Corporation. ROM 13 is used to store the operating system of the computer 10 as well as other proprietary programs, such as file directory routines. RAM 14 is utilized as the internal memory of the computer for accessing of data. The LCD display 15 with its associated video circuitry provides for the presentation of a display on a viewing screen. The crystal operated clock 16 provides for the necessary timing reference signals which are needed for the operation of computer 10. The battery 17 powers computer 10, permitting computer 10 to be a fully portable unit. Battery charger circuit 18 monitors the level of the battery 17 as well as charging the battery 17 when computer 10 is coupled to an external power source such as 110 Volts AC.

The I/O unit 19 interfaces with various I/O devices, such as keyboards and cursor control devices, such as a "mouse" or a trackball. The disk controller unit 20 is used to access a disk storage medium, such as a floppy disk. In computer 10, a hard disk is coupled and accessed by the parallel communications controller 23. The serial communication controller 21 and its drivers 22 are utilized to provide serial communication, such as supporting a RS-232 protocol. The sound circuits and drivers of sound unit 24 are utilized to

handshaking scheme wherein commands are provided by CPU 12 and replies are provided by PMGR 11 on data and handshake lines 33.

Once the command is sent from CPU 12 through via unit 28 to PMGR 11 and the handshake is completed, PMGR 11 decodes the command and executes it. If no reply data is to be returned, PMGR 11 waits for the handshake for the next command to begin from CPU 12. If reply data is to be returned, PMGR 11 begins the reply handshake and returns the requested data. In the preferred embodiment commands and replies are transmitted in a protocol comprising of a command/reply byte, a count byte and optional data bytes.

Once every 1/60 of a second (frequency of 60 Hz), the clock oscillator 16 generates an interrupt to PMGR 11 and this interrupt is coupled to CPU 12 on line 34. When this interrupt is generated, PMGR 11 closes the I/O channel from I/O controller 19 and further, will not respond to any handshake requests from CPU 12. The interrupt on line 34 causes CPU 12 to suspend the data transfer to PMGR 11. During this interrupt cycle, PMGR 11 performs its periodic monitoring routines which include updating the real time clock, checking the battery power level and sending an auto poll command. The auto poll command is associated with the auto poll scheme of the preferred embodiment in which the CPU 12, through PMGR 11, automatically interrogates (polls) devices coupled to bus 37 to determine the presence of data for transfer.

PMGR 11 contains the necessary I/O transceiver functions for transfer of information between PMGR 11 and I/O unit 19 on bus 37. Packets of information to be sent on bus 37 to I/O unit 19 are sent by CPU 12 to PMGR 11 in the data portion of the command signal. Data received by PMGR 11 from I/O controller 19 is buffered internally and once received, this data is stored within PMGR 11 until requested by CPU 12. If a new I/O command was transmitted by CPU 12 during a previous command/execution cycle, the new command and

computer 10 is disconnected from an external power source, PMGR 11 provides for a number of control and monitoring functions for this purpose. PMGR 11 is utilized to cause computer 10 to be in one of three separate modes of operation. The three modes are the normal, slow and sleep modes. PMGR 11 responds to each of these modes by controlling the clocking signal being sent to a given device and/or controlling the voltage being supplied to a given unit. The clock signals coupled from the clock oscillator 16 to PMGR 11 are coupled to the clock control unit 27. Clock control unit 27 operates as a switch to couple the various clock signals on lines 41, 42 and 43 to CPU 12, serial communication controller unit 21 and the disk controller unit 20, respectively.

A power supply 29, which receives its power from battery 17, provides the needed voltages by computer 10. These supply voltages, shown as Vcc's in Figure 1, are coupled through PMGR 11, wherein PMGR 11 provides separate Vcc sources to the various units through the analog interface unit 26. As shown in Figure 1, VccA is coupled to the CPU 12 and related units. Three other separate Vcc sources are also provided from PMGR 11 as dedicated Vcc voltages to serial communication drivers 22, sound unit 24 and to the modem 25 through analog interface unit 26. These voltages are designated as VccB, VccC and VccD, respectively. It is to be noted that control lines are also present between PMGR 11 and clock control unit 27 and between PMGR 11 and analog interface unit 26. In the preferred embodiment, analog interface unit 26 is comprised of a plurality of transistor switches for switching the various Vcc sources onto their corresponding lines. The clock control unit 27 also includes various switches for coupling the clock signals to the corresponding units. Further, it is to be appreciated that PMGR 11 also includes circuitry for the various clocking signals for distribution onto lines 41-43. It is to be noted that PMGR 11 can change the various clocking rates of the clocking signals present on lines 41-43.

memory then the transistor switch applying Vcc power to RAM 14 is kept closed so that Vcc is still applied to RAM 14 keeping it active in order to retain the stored information. It is to be noted that non-volatile memory is preferred so that Vcc need not be applied to RAM 14 in the sleep mode. Further, it is to be noted that the preferred embodiment uses CMOS memory.

In an alternative embodiment, VccA can be coupled onto line 45 in order to keep the power supplied to CPU 12. The internal clock of PMGR 11 can be decoupled from CPU 12 by clock control unit 27 thereby disabling the clock input to CPU 12 and halting the execution of the CPU. The CPU internal states are frozen with all CPU internal RAM and control registers remaining intact by halting the execution of the CPU. Halting the execution of CPU 12 typically will lower its power consumption by two orders of magnitude.

Although a number of conditions can cause computer 10 to wake from the sleep mode, computer 10 of the present invention has three possible conditions which triggers it to leave the sleep mode. PMGR 11 continues to monitor lines 37 such that any input from I/O controller19a will cause computer 10 to wake from the sleep state. The I/O input is typically a pressing of a key on the keyboard and/or the movement of the cursor control device. The second condition for waking up computer 10 occurs if the wake up timer (alarm clock) within PMGR 11 had been enabled and matches the real time clock within PMGR 11. Upon the activation of the alarm clock, PMGR wakes computer 10 from its sleep state. Finally, the third condition of computer 10 occurs if PMGR 11 was set to monitor the detection of a ring signal from modem 25. If an incoming signal is received by modem 25, the ring signal is detected by PMGR 11 and causes computer 10 to awake from its sleep state.

Upon waking, computer 10 accesses RAM 14 to retrieve the stored state of the various units for restoring computer 10 to the state it was in prior to

removed from this CMOS device, the device shuts down and consumes none or very little power. It is to be noted that in some of the devices, such as units 20 and 21, the clock signal can be decoupled from these devices while the Vcc supply to these devices are present.

Referring to Figure 3, a transistor switch 54 comprising one of the switches within analog interface unit 26 is shown. However, it is to be noted that a plurality of these switches reside within analog interface unit 26. One of the Vcc lines is coupled from PMGR 11 through transistor 55 to device 56. A control line also from PMGR 11 is coupled to the gate of transistor 55 for controlling the coupling of Vcc to device 56 through transistor 55. It is to be noted that power is supplied to device 56 when transistor 55 is made active and that device 56 may not necessarily be a CMOS device since power will be removed from device 56 when transistor 55 is cut off.

It is to be appreciated that the above description in reference to Figures 1-3 can be represented in various other circuit equivalent forms without departing from the spirit and scope of the invention. Further, in reference to Figure 1, the actual devices and the switching of the power and clock signals can be readily adapted to operate with other designs without departing from the spirit and scope of the present invention. However, in order to provide a more detailed workings of the present invention, various specific details pertaining tc the preferred embodiment are disclosed below. CPU 12 provides various commands to PMGR 11 for connecting the Vcc power to applicable devices as needed. Further, clock signals can be either disconnected from various devices, or in the alternative, PMGR 11 can provide different clock speeds, such as during the slow mode. CPU 12 can be made to provide these commands in response to a stored routine or in response to a monitoring function of the PMGR or in response to a user interaction through I/O unit 19.

In reference to the battery charger circuit 18, the circuit charges the battery when coupled to an external power source, but circuit 18 is also utilized to monitor battery 17. PMGR 11 monitors the power level of battery 17 and alerts the user when that level drops to a predetermined level, permitting the user to finish the current job of the computer and shutting down the computer prior to complete breakdown of computer 10. An analog-to-digital converter within PMGR11 provides for the conversion of the analog battery voltage to a digital signal. Although not shown in Figure 1, a temperature sensing mechanism is also coupled to a PMGR 11 to sense the temperature and another analog-to-digital converter within PMGR 11 is also used to convert this analog signal to a digital signal.

It is to be appreciated that the PMGR 11 of the preferred embodiment of the present invention provides for a variety of techniques to monitor and control the distribution of power and clocking signals in order to conserve the time that computer 10 can be self-sustaining when decoupled from an external power source.

3. The apparatus of Claim 2, wherein said second switching means decouples said clock signal from each of various units coupled to said second switching means until each of said respective units are needed to be accessed by said CPU.

4. The apparatus of Claim 3, wherein said control means provides for three modes of operation, a first mode for providing power and clock signals to said various units when needed by said computer, a second mode for removing power or clock signal to deactivate respective devices to conserve power, and a third state in which the frequency of said clock signal is reduced in order to reduce power consumption to those units coupled to receive said clock signal.

5. In a portable computer, having a central processing unit (CPU), a memory, a plurality of peripheral devices including a user interactive device, and a battery for powering said computer, an apparatus for managing the use of power from said battery by said computer, comprising:

control means coupled to said CPU for receiving commands from said CPU and also coupled to receive inputs from said user interactive device;

said control means also coupled to said battery for controlling distribution of said power to various units of said computer;

said control means also coupled to provide an internal clock and distributing a clock signal to some of said units of said computer;

said control means providing for three modes of operation of said computer, an active mode for providing active operation of said computer, a sleep mode for placing said computer in an inactive state to conserve power and a slow mode in which the frequency of said clock signal is reduced in

9. The apparatus of Claim 8, wherein said computer enters its sleep mode if an input from an input/output (I/O) device does not occur for a first predetermined time period.

10. The apparatus of Claim 9, wherein said monitoring means monitors said I/O device and causes said computer to leave its sleep mode if an input is sensed from said I/O device.

11. The apparatus of Claim 10, wherein said computer enters its slow mode if said input from said I/O device does not occur for a second predetermined time period, said second predetermined time period being shorter than said first predetermined time period.

12. The apparatus of Claim 11, wherein said monitoring means monitors said I/O device and causes said computer to leave its sleep mode if an input is sensed from a modem coupled to said control means.

13. The apparatus of Claim 12, wherein said I/O device is said user interactive device.

14. The apparatus of Claim 10, wherein said first and second switches are field-effect transistors.

15. The apparatus of Claim 14 further including a reference clock means coupled to said control means for providing a crystal controlled reference clock signal.